

IPW



PTO/SB/21 (02-04)

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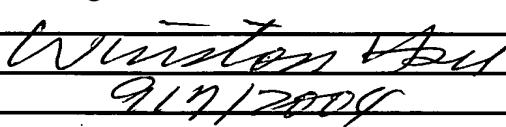
(to be used for all correspondence after initial filing)

	Application Number	10/710,669	
	Filing Date	07/28/2004	
	First Named Inventor	Weng, Yi-Tang	
	Art Unit		
	Examiner Name		
Total Number of Pages in This Submission	21	Attorney Docket Number	NANP0001USA

### ENCLOSURES (Check all that apply)

<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance communication to Technology Center (TC)
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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<input type="checkbox"/> After Final	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Proprietary Information
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<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		
Remarks		

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Winston Hsu, Reg. No.: 41,526	
Signature		
Date	9/7/2004	

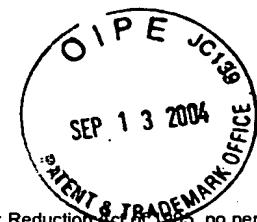
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PTO/SB/17 (10-03)

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# FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

Applicant claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** (\$0.00)

**Complete if Known**

Application Number	10/710,669
Filing Date	07/28/2004
First Named Inventor	Weng, Yi-Tang
Examiner Name	
Art Unit	
Attorney Docket No.	NANP0001USA

**METHOD OF PAYMENT (check all that apply)**

Check  Credit card  Money Order  Other  None

**Deposit Account:**

Deposit Account Number  
Deposit Account Name

50-3105

North America Intellectual Property Corp.

The Director is authorized to: (check all that apply)

Charge fee(s) indicated below  Credit any overpayments  
 Charge any additional fee(s) or any underpayment of fee(s)  
 Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

**FEES CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 770	2001 385	Utility filing fee	
1002 340	2002 170	Design filing fee	
1003 530	2003 265	Plant filing fee	
1004 770	2004 385	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	
<b>SUBTOTAL (1)</b>		<b>(\$0.00)</b>	

**2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE**

Total Claims	Extra Claims	Fee from below	Fee Paid
	-20** =	X =	=
Independent Claims	- 3** =	X =	=
Multiple Dependent			=

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 18	2202 9	Claims in excess of 20
1201 86	2201 43	Independent claims in excess of 3
1203 290	2203 145	Multiple dependent claim, if not paid
1204 86	2204 43	** Reissue independent claims over original patent
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent
<b>SUBTOTAL (2)</b>		<b>(\$0.00)</b>

\*\*or number previously paid, if greater. For Reissues, see above

**3. ADDITIONAL FEES**

Large Entity	Small Entity	Fee Description	Fee Paid
Fee Code (\$)	Fee Code (\$)		
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	1053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for ex parte reexamination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 420	2252 210	Extension for reply within second month	
1253 950	2253 475	Extension for reply within third month	
1254 1,480	2254 740	Extension for reply within fourth month	
1255 2,010	2255 1,005	Extension for reply within fifth month	
1401 330	2401 165	Notice of Appeal	
1402 330	2402 165	Filing a brief in support of an appeal	
1403 290	2403 145	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,330	2453 665	Petition to revive - unintentional	
1501 1,330	2501 665	Utility issue fee (or reissue)	
1502 480	2502 240	Design issue fee	
1503 640	2503 320	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	1806 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (times number of properties)	
1809 770	2809 385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 770	2810 385	For each additional invention to be examined (37 CFR 1.129(b))	
1801 770	2801 385	Request for Continued Examination (RCE)	
1802 900	1802 900	Request for expedited examination of a design application	
Other fee (specify) _____			
*Reduced by Basic Filing Fee Paid			
<b>SUBTOTAL (3)</b>		<b>(\$0.00)</b>	

(Complete if applicable)

Name (Print/Type)	Winston Hsu	Registration No. (Attorney/Agent)	41,526	Telephone	886289237350
Signature					
Date	9/27/2004				

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PTO/SB/08A (08-03)

Substitute for form 1449/PTO		<b>Complete if Known</b>	
		Application Number	10/710,669
		Filing Date	07/28/2004
		First Named Inventor	Weng, Yi-Tang
		Art Unit	
		Examiner Name	
Sheet	1	of	1
		Attorney Docket Number	NANP0001USA

## **U. S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

<b>Examiner Signature</b>		<b>Date Considered</b>	
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<sup>1</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>2</sup>Applicant's unique citation designation number (optional). <sup>3</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>4</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>5</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>6</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>7</sup>Applicant is to place a check mark here if English language Translation is attached.

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**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

5 Applicants: Weng, Yi-Tang

Filing Date: 07/28/2004

Serial No.: 10/710,669

Docket No.: NANP0001USA

10 Title: METHOD FOR FABRICATING A PACKAGING SUBSTRATE

To: Commissioner for Patents

P.O. BOX 1450

Alexandria, VA 22313-1450

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Subject: Information disclosure statement under 37C.F.R.§1.56.

Dear Sir/Madame:

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This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. §1.56. The Applicant wishes to make of record the document listed on the accompanying form PTO/SB/08A. It is respectfully requested that the Examiner initials the cited reference 25 on the form and that it be made of record in the application and that a copy of the initialed form be sent to the Applicant with the next communication from the Examiner. Since the IDS is filed before the mailing of a first Office action on the merits, a petition to request consideration of the information disclosure statement is hereby requested according to 37 CFR §1.97(b).

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To comply with 37 C.F.R.§1.98, the Applicant hereby respectfully submits a copy of the cited reference (Taiwan Patent Pub. No. 538,512), and a concise explanation of

the relevance.

Taiwan Patent Pub. No. 538,512 discloses a method for manufacturing a packaging substrate utilizing stacked photoresist during image transferring. As shown in Fig.1A, copper films 11 are first laminated on a core 10. As shown in Fig.1B, first image transfer process is carried out to form a photoresist 12 that defines a copper coating area A. As shown in Fig.1C, a copper layer 13 is then plated into the copper coating area A to form conductive wire pattern. As shown in Fig.1D, a second patterned photoresist 14 is stacked onto the photoresist 12. The second patterned photoresist 14 defines Ni/Au-plating area B of the pad 15. A Ni/Au layer 16 is then plated into the Ni/Au-plating area B, as shown in Fig.1E. Subsequently, the photoresist 12 and photoresist 14 are removed simultaneously. As shown in Fig.1G, the copper films 11 that are not covered by the formed pattern are etched away. Finally, as shown in Fig.1H, patterned solder mask is formed thereon.

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As described in the Background of the specification of the present application, the prior art method disclosed in Taiwan Patent Pub. No. 538,512 encounters a Ni/Au overhang problem due to that the sidewalls of the contact pad are not covered by the Ni/Au layer (can be explicitly seen through Fig.1G~Fig.1H). The exposed sidewalls of the contact pads may be oxidized resulting in short circuiting or reliability concerns.

According to the claimed invention of the present application, a method for fabricating a packaging substrate is disclosed. A carrier plate having thereon at least one thin copper base layer is prepared. A first patterned photoresist layer is then formed on the thin copper base layer, the first patterned photoresist layer has a recessed trench area defining a copper circuit pattern. Copper is electroplated into the recessed trench area to form the copper circuit pattern. The first patterned photoresist layer is then removed. Thereafter, a second patterned photoresist layer exposing an Au-plating area of the copper circuit pattern is formed. The thin copper base layer exposed by the second patterned photoresist layer is etched away. A third patterned photoresist layer is formed on the second patterned photoresist layer to mend a recess under the second patterned photoresist layer. Using the third patterned photoresist

layer as an electroplating mask, a conventional electroplating process is performed to electroplate a metal layer onto the copper circuit pattern in the Au-plating area. The second and third patterned photoresist layers are removed. The remaining thin copper base layer being exposed after stripping the second and third patterned photoresist  
5 layers is then removed.

The present invention comprises at least the following advantages. First, the cost per substrate is reduced since there is no need to coat an additional conductive metal layer for electroplating after the definition of circuit pattern layout. The conductive  
10 materials used to assist electroplating include the thin copper base layer and the chemically deposited copper layer. The potential scratch or collision damages can be effectively prevented since the entire circuit pattern is revealed at a later fabrication stage. Further, metal peeling is avoided thereby promoting the production yield. Moreover, sidewalls of the circuit pattern in the Au-plating area are also covered by  
15 Ni/Au film and thus avoiding overhang problem.

It is therefore believed that the claimed invention of the present application is substantially different from the prior art Taiwan Patent Pub. No. 538,512. For convenience, Claim 1 of the present application is listed below:

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Claim 1 A method for fabricating a packaging substrate, comprising:

providing a carrier plate having thereon at least one thin copper base layer;

forming a first patterned photoresist layer on said thin copper base layer, said first patterned photoresist layer has a recessed trench area defining a copper circuit  
25 pattern;

electroplating copper in said recessed trench area to form said copper circuit pattern including a to-be-Au-plating area that has a larger surface area as the terminal of said copper circuit pattern;

stripping said first patterned photoresist layer;

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forming a second patterned photoresist layer exposing said to-be-Au-plating area of said copper circuit pattern;

using said second patterned photoresist layer as an etching hard mask, etching

away said thin copper base layer exposed by said second patterned photoresist layer and said to-be-Au-plating area;

forming a third patterned photoresist layer on said second patterned photoresist layer to mend a recess under said second patterned photoresist layer;

5 using said third patterned photoresist layer as an electroplating mask, electroplating a metal layer onto said copper circuit pattern in said to-be-Au-plating area;

stripping said second and third patterned photoresist layers; and

10 etching away remaining said thin copper base layer being exposed after stripping said second and third patterned photoresist layers.

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Respectfully Submitted,

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Winston Hsu

Date: 9/19/2004

Winston Hsu, Patent Agent No. 41,526

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